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Joseph A Walkowski
TraskBritt PC
P O Box 2550
Salt Lake City, UT 84110

EXAMINER	
TRAN, TRANG U	
ART UNIT	**PAPER NUMBER**
2614	22

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/048,933	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Trang U. Tran	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 24, 2003 have been fully considered but they are not persuasive.

In re pages 6-9, applicant argues that, with respect to claim 1, Dea and So do not appear to teach or suggest "receiving a current video frame at a core logic chip...from a video source originating the video frame...the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus; computing at the core logic chip the difference frame...as the current video frame streams into the core logic chip...the difference frame including computing the difference frame in the core logic chip...; storing the difference frame in the system memory...; and the host retrieving the difference frame directly from the system memory via the core logic chip to complete compression of the video data" because the frame difference block 220 of Dea can only be fed frame data for calculating a difference frame from data that has been stored in memory 114 and not, as claimed by Applicant, by "receiving a current video frame at a core logic chip...from a video source originating the video frame...the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" and "computing at the core logic chip the difference frame...as the current video frame streams into the core logic chip...the difference frame including computing the difference frame in the core logic chip..." and that any rejection of the presently claimed invention based upon any combination of the Dea reference and the So reference under 35 U.S.C. § 103

would be a hindsight reconstruction of the presently claimed invention based solely upon the Applicants' disclosure because there is no suggestion or teaching whatsoever in the cited prior art for any modification thereof to yield the presently claimed invention but, solely, Applicants' own disclosure.

In response, the examiner respectfully disagrees. First at all, Dea discloses in col. 5, lines 38-52 that "Data transmitting by way of **data bus 118** of remote video interface system 100 is received by **accelerator bus interface 200** of **compression/decompression accelerator 120**.... for filtering prior to being applied to **frame difference block 220** depending...a three stage adder and feedback". From the above passages it is clear that the core logic chip (compression/decompression accelerator 120) of Dea is "receiving a current video frame at a core logic chip ... from a video source (data bus 118) originating the video frame...the core logic chip for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" and "computing (the frame difference block 220) at the core logic chip the difference frame...as the current video frame streams into the core logic chip...the difference frame including computing the difference frame in the core logic chip..." Thus, Dea does indeed disclose the alleged claimed limitations of claim 1.

Finally, the examiner has pointed out in the last Office Action what each of the prior art references teaches and has indicated how and why these references would have been combined to arrive at the claimed invention. Applicant cannot show non-obviousness by attacking the references individually where, as here, the rejection is based on a combination of references. In re Keller, 642 F.2d 413, 208 USPQ 871

(CCPA 1981). So was cited only to suggest the conventional well-known North Bridge chip. Applicant do not credibly argue, nor could him, that it would have been unobvious to incorporate the well known North Bridge chip into Dea's system. The examiner believes that the artisan would have recognized the obviousness of the well-known North Bridge chip of So and would have combined the references as proposed by the examiner.

In re page 9, applicant states that dependent claims 2-3, 5-7 and 12 are allowable for the same reasons as discussed in independent claim 1 above.

In response, as discussed above with respect to claim 1, the combination of Dea and So shows all the claimed limitations.

In re pages 9-12, applicant argues that claims 4, 9, 13-17 and 19 are allowable for the same reasons as discussed in independent claim 1 above.

In response, as discussed above with respect to claim 1, the combination of Dea and So shows all the alleged limitations.

In re pages 12-13, applicant argues that claim 8 is allowable for the same reasons as discussed in independent claim 1 above.

In response, as discussed above with respect to claim 1, the combination of Dea and So shows all the alleged limitations.

In re pages 13-14 applicant argues that claim 18 is allowable for the same reasons as discussed in independent claim 1 above.

In response, as discussed above with respect to claim 1, the combination of Dea and So shows all the alleged limitations.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-7, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea `208 in view of So `559 (both of record).

Considering claim 1 (Four Time Amended), Dea discloses a remote video processing system including compression/decompression accelerator. Dea discloses the following claimed subject matter, note:

a) the claimed method for compressing video data in a computer system is met by the description at column 4, lines 36-41 and lines 17-19, and FIG. 1, where of the described compression/decompression accelerator 120 performs the compression method;

b) the claimed step of receiving a current video frame at a core logic chip in the computer system from a video source originating the video frame is met by description at column 6, lines 42-44 and FIG. 2;

c) the teaching of " the computer system including the core logic unit for coupling a processor to a system memory and for coupling the processor and the system memory to a system bus" which is described and depicted on Fig. I and column 4, lines 37-60, where as Fig. 1 depicts the compress/decompression accelerator 120

(core logic unit) is coupled to processor 112 and DRAM 114 (system memory) through the data and system bus 116, 118;

d) the claimed step of computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the core logic chip is met by the description of the subtraction function of frame difference block 220 column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2);

e) the claimed step of storing difference frame in the system memory in the computer system which is met by memory 114 as described at column 9, line 60 to column 10, line 3, column 11, lines 1-13 and FIG. 2, whereas the passage bridging from column 9 and 10 describes the frame difference encoding data by the encoder block 246 is first stored in the buffer 248, and the passage from column 11 further discloses the run/value pairs from the encoder 246 are applied to the encode output circular buffer 332, in which the buffer 332 may located in DRAM memory 114 ;

f) the teaching of " the difference frame includes computing the difference frame in a core logic unit within the computer system" as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 1, 2); and

g) the teaching of "the processor retrieving the difference frame directly from the system memory via the core logic unit to complete compression of the video data which as described at column 11, lines 19-33.

However, Dea does not explicitly teach the claimed computing the difference frame in core logic chip, wherein the core logic chip is a north bridge chip as recited, in stead Dea teaches the use of the core logic unit as described above. Nonetheless, Dea teaches the computing the difference frame in a compression/depression accelerator 120 (core logic unit) as discussed above in points (c), (f) and (g).

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator the is provided either at the North bridge or AGP graphic/video chip as described at column 17, lines 24-29. It is noted that So also discloses that accelerator (core logic unit) is provided at the North Bridge Chip, and whereas such implementation which has the advantage of achieving MIPS (millions of instructions per second) column 4, lines 14-16 without substantially loading the PCI (peripheral component interface) bus (column 17, lines 2432).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video accelerator (core logic unit) with the teaching of graphic accelerator that is provided either at the North bridge chip for the stated advantage.

Considering claim 2(Amended), the claimed storing the current video frame in the system memory in the computer system which is met by memory 114 as described at column 9, line 60 - column 10, line 3, column 11, lines 1-13 and FIG. 2, whereas the passage bridging from column 9 and 10 describes the frame difference encoding data by the encoder block 246 is first stored in the buffer 248, and the passage from column

11 further discloses the run/value pairs from the encoder 246 are applied to the encode output circular buffer 332, in which the buffer 332 may located in DRAM memory 114.

Considering claim 3 (Amended), the claimed wherein the current video frame is written over a previous video frame in the memory which is met by the DRAM 114 (at column 9, line 60 - column 10, line 3, column 11, lines 1-13 and FIG. 2.), whereas the DRAM 114 receives video frame sequentially that the area stores the previous video frame is subsequently replace by the newly received current video frame.

Considering claim 5, the claimed step of computing a difference between a block of data from the current video frame and a. block of data from the previous video frame is met description at column 10, lines 53-56 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 described the utilizing of the block of data from the current and previous video frame.

Considering claim 6 (Amended), the claimed wherein storing the difference frame in memory includes storing the differences frame in the system memory using block transfer which is met by the description at column 10, line 53 - column 11, line 7 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 and 11 described the utilizing of the block of data from the current and previous video frame and subsequently recognized that data stored in buffer is in the from of block computer system is met by the processor 112 and the compression/decompression accelerator 120 (FIG. 2).

4. Claims 4, 9, 13-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea `208 (of record) and So `559(New), and further in view of Abramatic et al. `383 (of record).

Considering claim 4, the system of Dea and So discloses the claimed invention except for the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame.

Nonetheless, Dea teaches that a step of computing the difference frame between the current video frame and the previous video frame as discuss above in claim 1.

Furthermore, Abramatic et al. teaches that a form of image compression consists the detecting variations (difference) between one image and the next one as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teaches that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidate at column 7, lines 32-35.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the Dea and So combination with such teachings for the stated advantage.

Considering claim 9, the system of Dea and So discloses the claimed invention except for the claimed using the video data in compressed form in a video teleconferencing system. Since examiner takes Official Notices that it is notoriously well-known in the art for the usage of the compressed video data format in a teleconference system, whereof the compressed video data format transmission provides the benefit of bandwidth conservation on the communication medium. Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Dea and So accordingly, in order to facilitate the video teleconferencing functionality and to make efficient use of the bandwidth on the communication link.

Considering claim 13(Four-times Amended), Dea discloses a remote video processing system including compression/decompression accelerator. Dea discloses the following claimed subject matter, note:

a) the claimed method for compressing video data in a computer system is met by the description at column 4, lines 36-41 and lines 17-19, and FIG. 1, where of the described compression/decompression accelerator 120 performs the compression method;

b) the claimed step of receiving a current video frame at a core logic chip in the computer system from a video source originating the video frame is met by description at column 6, lines 42-44 and FIG. 2;

c) the teaching of " the computer system including the core logic unit for coupling a processor to a system memory and for coupling the processor and the

system memory to a system bus" which is described and depicted on Fig. 1 and column 4, lines 37-60, where as Fig. 1 depicts the compress/decompression accelerator 120 (core logic unit) is coupled to processor 112 and DRAM 114 (system memory) through the data and system bus 116, 118;

d) the claimed step of computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the core logic chip is met by the description of the subtraction function of frame difference block 220 column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2);

e) the claimed step of storing difference frame in the system memory in the computer system which is met by the description of memory 114 as described at column 9, line 60 - column 10, line 3, column 11, lines 1-13 and FIG. 2, whereas the passage bridging from column 9 and 10 describes the frame difference encoding data by the encoder block 246 is first stored in the buffer 248, and the passage from column1 further discloses the run/value pairs from the encoder 246 are applied to the encode output circular buffer 332, in which the buffer 332 may located in DRAM memory 114 the claimed storing the current video frame in the memory in the computer system is met by the current frame memory 204 (column 6, lines 42-44, and FIG. 2);

f) the claimed step of storing the current video frame in the system memory in the computer system which is met by memory 114 as described at column 29, lines 63-65, whereas the decoded image block is considered as the current video frame that is written to the memory 114;

g) the teaching of "the processor retrieving the difference frame directly from the system memory via the core logic unit to complete compression of the video data which as described at column 11, lines 19-33; and

h) the claimed step of compressing the video data using the difference frame to produce compressed video data is met by the description of FIG. 3A and column 10, line 53 - column 11, line 7, whereof FIG. 3A depicted the frame difference block 220 provides a difference frame and subsequently after the variable length encoding block , the compressed video bitstream 338 is output.

However, Dea does not explicitly disclose, note

i) the claimed computing the difference frame in a core logic chip , wherein the core logic chip is a north bridge chip as recited;

ii) the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame;

Regarding (i), Dea teaches the computing the difference frame in a compression/depression accelerator 120 (core logic unit) as discussed above in points (g) and (h).

So discloses an integrated circuit provides on a single chip for use with a first processor off-chip. So discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator that is provided either at the north bridge or AGP graphic/video chip as described at column 17, lines 24-29. It is noted that So discloses that accelerator (core logic unit) is provided at the North Bridge Chip, and So further discloses such implementation which has the advantage of achieving MIPS (millions of

instructions per second, column 4, lines 14-16) without substantially loading the PCI (peripheral component interface) bus (column 17, lines 24-32).

Therefore the examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Dea's teaching of video accelerator (core logic unit) with the teaching of graphic accelerator the is provided either at the North bridge chip for the stated advantage.

Regarding (ii), Dea teaches a step of computing the difference frame between the current video frame and the previous video frame as discuss above at point (c) above.

Furthermore, Abramatic et al. teaches that a form of video compression consists in detecting variations (difference) between on image and the next as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teaches that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidate at column 7, lines 32-35.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to modify the system of Dea and So in combination with such teachings for the intended advantage.

Considering claim 14(Amended), the claimed wherein the current video frame is written over a previous video frame in the memory which is met by the DRAM 114 (at column 9, line 60 - column 10, line 3, column 11, lines 1-13 and FIG. 2), whereas the DRAM 114 receives video frame sequentially that the area stores the previous video frame is subsequently replace by the newly received current video frame.

Considering claim 15, the claimed step of computing a difference between a block of data from the current video frame and a block of data from the previous video frame is met description of Dea at column 10, lines 53-56 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 described the utilizing of the block of data from the current and previous video frame.

Considering claim 16 (Amended), the claimed wherein storing the difference frame in memory includes storing the differences frame in the system memory using block transfer which is met by the description at column 10, line 53 - column 11, line 7 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 and II described the utilizing of the block of data from the current and previous video frame and subsequently recognized that data stored in buffer is in the from of block.

Considering claim 17, the system of Dea and So discloses the claimed invention except for the claimed limitation of using the video data in compressed form in a video teleconferencing system. Since examiner takes Official Notices that it is notoriously well-known in the art for the usage of the compressed video data form in a teleconference system, whereof the compressed video data format transmission provides the benefit of bandwidth conservation on the communication linking medium.

Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the Dea and So system accordingly in order to facilitated the video teleconferencing and to make efficient use of the bandwidth on the communication link.

Considering claim 19(Amended), the system of Dea, So and Abramatic et al. discloses the claimed invention except for the claimed step of storing instruction and data for the computer system in the system memory. Dea teaches a step of storing data for the computer system in the memory as the description of DRAM 114 at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Examiner takes Official Notice that it is both notoriously well-known in the art to integrate video processing systems in computer systems, and to consolidate storage for disparate processes in common memories. Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Dea and So accordingly in order to provide a computer backbone to facilitate the video processing and to make efficient use of memory storage capacity for both the data and executable instructions.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea `208 and So `559 (New) as applied to claim 1 above, and further in view of Hardiman ` 223 (of record).

Considering claim 8, the system of Dea and So discloses the claimed invention except for the claimed step of performing a color space conversion on the video data.

Hardiman discloses an invention relates to compression coding of a video program. Hardiman disclose the claimed performing a color space conversion on the video data is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and Fig. 2). Hardiman discloses that by implementing the color space conversion on video data provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57). The examiner submits that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Dea and So by using the color space conversion circuit as taught by Hardiman for the stated benefit.

6. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea `208, So `559 and Abramatic et al. `383 (all of Record) as applied to claim13 above, and further in view of Hardiman `223.

Considering claim 18, the system of Dea, So and Abramatic et al. discloses the claimed invention except for the claimed step of performing a color space conversion on the video data. Hardiman discloses an invention that relates to compression coding of a video program. Hardirnan disclose the claimed performing a color space conversion on the video data is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2). Hardiman discloses that by implementing the color space conversion on video data provides the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57). The examiner submits that it would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the systern of Dea, So and Abramatic et al. by using the color space conversion circuit as taught by Hardiman for the stated benefit.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trang U. Tran** whose telephone number is **(703) 305-0090.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John W. Miller,** can be reached at **(703) 305-4795.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 308-HELP.

TT TT
January 24, 2004

MICHAEL H. LEE
PRIMARY EXAMINER